

**CLAIMS**

What is claimed is:

1. A method for transmitting a loopback cell within a  
2 switching node of an ATM connection, said switching node  
3 including a first adapter having associated ports and a  
4 second adapter having associated ports, wherein said  
5 loopback cell enters said switching node by a first  
6 adapter port, said method comprising:

detecting a loopback condition when an ATM cell  
enters said first adapter; and

in response to a loopback condition:

10 appending a routing label to said ATM cell  
11 indicating that said ATM cell is a loopback cell to be  
12 looped back on said ATM connection; and

13 transferring said loopback cell to said first  
14 adapter port utilizing said appended routing  
15 label.

1. The method of claim 1, wherein said appending step  
2 is preceded by the step of identifying said ATM cell  
3 within said first adapter.

1. The method of claim 2, wherein said identifying said  
2 ATM cell is performed with respect to said first adapter  
3 port and a virtual path/virtual circuit encoded on said  
4 ATM cell.

1       4. The method of claim 1, wherein said detecting step  
2       comprises reading a loop condition bit from a dedicated  
3       register.

1       5. The method of claim 1, wherein said transferring  
2       step further comprises:

3               switching said ATM cell to said second adapter from  
4       said first adapter; and

5               switching said ATM cell back to said to said first  
6       adapter from said second adapter.

1       6. The method of claim 1, wherein said routing label is  
2       appended to said loopback cell only if a loop control bit  
3       is set by a control point of said switching node within  
4       said first adapter.

1       7. The method of claim 6, further comprising, in  
2       response to a loopback condition, setting said loop  
3       control bit within said first adapter.

1       8. The method of claim 6, further comprising adding a  
2       loopback flag to said loopback cell if said loop control  
3       bit is set, wherein said loopback flag serves as an  
4       indicator for a protocol engine within said first adapter  
5       that said routing labels have to be appended to said  
6       loopback cell.

9. The method of claim 1, wherein said routing label includes a switch routing label for identifying said first adapter as the output adapter from which said loopback cell will exit said switching node.

10. The method of claim 1, wherein said routing label includes a protocol engine correlator for pointing to a connection control block within said first adapter.

11. The method of claim 1, wherein the ATM header virtual path/virtual circuit of said loopback cell is not swapped by the protocol engine of said first adapter before said loopback cell is transmitted over said ATM network by said first adapter port.

1       12. A system for transmitting a loopback cell within a  
2       switching node of an ATM connection, said switching node  
3       including a first adapter having associated ports and a  
4       second adapter having associated ports, wherein said  
5       loopback cell enters said switching node by a first  
6       adapter port, said system comprising:

7               processing means within said switching node for  
8       detecting a loopback condition when an ATM cell enters  
9       said first adapter;

10              a routing header function for appending a routing  
11       label to said ATM cell indicating that said ATM cell is a  
12       loopback cell to be looped back on said ATM connection;  
13       and

14              a switching engine for transferring said loopback  
15       cell to said first adapter port utilizing said appended  
16       routing label.

17. The system of claim 12, further comprising an ATM  
18       label lookup table for identifying said ATM cell within  
19       said first adapter.

20. The system of claim 12, further comprising  
21       processing means for reading a loop condition bit from a  
22       dedicated register.

23. The system of claim 12, wherein said routing label  
24       is appended to said loopback cell only if a loop control  
25       bit is set by a control point of said switching node  
26       within said first adapter.

1       16. The system of claim 15, further comprising  
2       processing means for setting said loop control bit within  
3       said first adapter.

1       17. The system of claim 15, further comprising  
2       processing means for adding a loopback flag to said  
3       loopback cell if said loop control bit is set, wherein  
4       said loopback flag serves as an indicator for a protocol  
5       engine within said first adapter that said routing labels  
6       have to be appended to said loopback cell.

1       18. The system of claim 12, wherein said routing label  
2       includes a switch routing label for identifying said  
3       first adapter as the output adapter from which said  
4       loopback cell will exit said switching node.

1       19. The system of claim 12, wherein said routing label  
2       includes a protocol engine correlator for pointing to a  
3       connection control block within said first adapter.

1       20. The system of claim 12, wherein the ATM header  
2       virtual path/virtual circuit of said loopback cell is not  
3       swapped by the protocol engine of said first adapter  
4       before said loopback cell is transmitted over said ATM  
5       network by said first adapter port.